FAIRCHILD SEMICONDUCTOR™

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74VCXR162601
Low Voltage 18-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in the Outputs

General Description

The VCXR162601, 18-bit universal bus transceiver, combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH-to-LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. Output-enable $\overline{OEAB}$ is active-LOW. When $\overline{OEAB}$ is HIGH, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA and $\overline{CLKENBA}$.

The 74VCXR162601 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V. The VCXR162601 is also designed with 26Ω series resistors on both the A and B Port outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

Features

- 1.4V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors on both the A and B Port outputs.
- t_{PD} (A to B, B to A)
  3.8 ns max for 3.0V to 3.6V V_{CC}
- Power-down HIGH impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
  ±12 mA @ 3.0V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
  Human body model > 2000V
  Machine model >200V

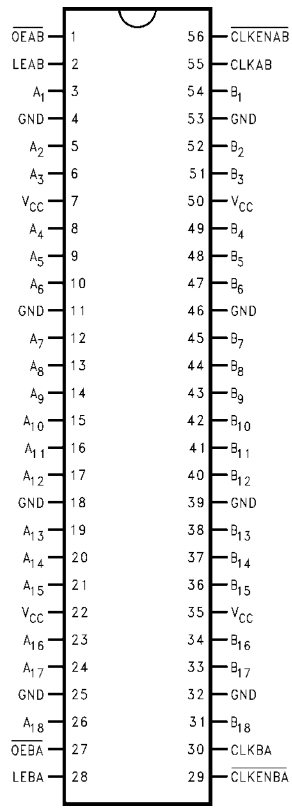
Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74VCXR162601MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable Inputs (Active LOW)
LEAB, LEBA	Latch Enable Inputs
CLKAB, CLKBA	Clock Inputs
$\overline{CLKENAB}$, $\overline{CLKENBA}$	Clock Enable Inputs
A_1–A_{18}	Side A Inputs or 3-STATE Outputs
B_1–B_{18}	Side B Inputs or 3-STATE Outputs

Function Table (Note 2)

Inputs					Outputs
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	A_n	B_n
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0 (Note 3)
H	L	L	X	X	B_0 (Note 3)
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0 (Note 3)
L	L	L	H	X	B_0 (Note 4)

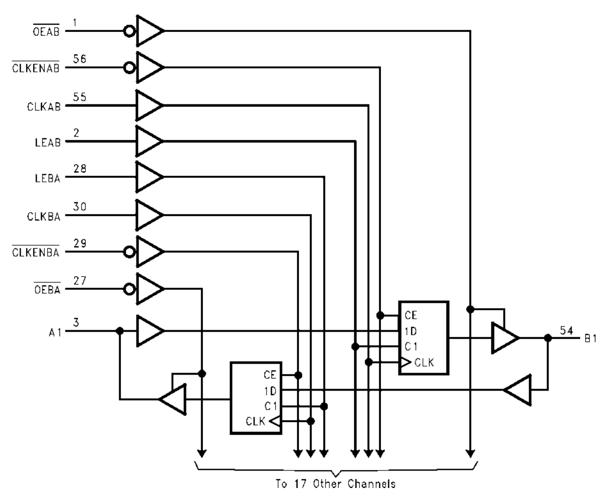
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = HIGH Impedance

Note 2: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

Note 3: Output level before the indicated steady-state input conditions were established

Note 4: Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

Logic Diagram



Absolute Maximum Ratings (Note 5)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATED	−0.5V to +4.6V
Outputs Active (Note 6)	−0.5 to V_{CC} + 0.5V
DC Input Diode Current (I_{IK}) V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or Ground)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 7)

Power Supply	
Operating	1.4V to 3.6V
Input Voltage	−0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±12 mA
V_{CC} = 2.3V to 2.7V	±8 mA
V_{CC} =1.65V to 2.3V	±3 mA
V_{CC} = 1.4V to 1.6V	±1 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 5: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	0.65 x V_{CC}		
			1.4 - 1.6	0.65 x V_{CC}		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		0.35 x V_{CC}	
			1.4 - 1.6		0.35 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.7 - 3.6	V_{CC} - 0.2		V
		I_{OH} = −6 mA	2.7	2.2		
		I_{OH} = −8 mA	3.0	2.4		
		I_{OH} = −12 mA	3.0	2.2		
		I_{OH} = −100 µA	2.3 - 2.7	V_{CC} - 0.2		
		I_{OH} = −4 mA	2.3	2.0		
		I_{OH} = −6 mA	2.3	1.8		
		I_{OH} = −8 mA	2.3	1.7		
		I_{OH} = −100 µA	1.65 - 2.3	V_{CC} - 0.2		
		I_{OH} = −3 mA	1.65	1.25		
		I_{OH} = −100 µA	1.4 - 1.6	V_{CC} - 0.2		
		I_{OH} = −1 mA	1.4	1.05		

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.7 - 3.6		0.2	V
		I_{OL} = 6 mA	2.7		0.4	
		I_{OL} = 8 mA	3.0		0.55	
		I_{OL} = 12 mA	3.0		0.8	
		I_{OL} = 100 µA	2.3 - 2.7		0.2	
		I_{OL} = 6 mA	2.3		0.4	
		I_{OL} = 8 mA	2.3		0.6	
		I_{OL} = 100 µA	1.65 - 2.3		0.2	
		I_{OL} = 3 mA	1.65		0.3	
		I_{OL} = 100 µA	1.4 - 1.6		0.2	
		I_{OL} = 1 mA	1.4		0.35	
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	1.4 - 3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or V_{IL}	1.4 - 3.6		±10.0	µA
I_{OFF}	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10.0	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	1.4 - 3.6		20.0	µA
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 8)	1.4 - 3.6		±20.0	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 - 3.6		750	µA

Note 8: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Max	Units	Figure Number
f_{MAX}	Maximum Clock Frequency	$C_L = 30$ pF	3.3 ± 0.3	250		MHz	
			2.5 ± 0.2	200			
			1.8 ± 0.15	100			
		$C_L = 15$ pF	1.5 ± 0.1	80.0			
t_{PHL}, t_{PLH}	Propagation Delay A to B or B to A	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.6	3.8	ns	Figures 1, 2
			2.5 ± 0.2	0.8	4.6		
			1.8 ± 0.15	1.5	9.2		
		$C_L = 15$ pF, $R_L = 2k\Omega$	1.5 ± 0.1	1.0	18.4		Figures 7, 8
t_{PHL}, t_{PLH}	Propagation Delay Clock to A or B	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.6	4.4	ns	Figures 1, 2
			2.5 ± 0.2	0.8	5.5		
			1.8 ± 0.15	1.5	9.8		
		$C_L = 15$ pF, $R_L = 500\Omega$	1.5 ± 0.1	1.0	19.6		Figures 7, 8
t_{PHL}, t_{PLH}	Propagation Delay LEBA or LEAB to A or B	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.6	4.4	ns	Figures 1, 2
			2.5 ± 0.2	0.8	5.8		
			1.8 ± 0.15	1.5	9.8		
		$C_L = 15$ pF, $R_L = 500\Omega$	1.5 ± 0.1	1.0	19.6		Figures 7, 8
t_{PZL}, t_{PZH}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.6	4.3	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	5.9		
			1.8 ± 0.15	1.5	9.8		
		$C_L = 15$ pF, $R_L = 2k\Omega$	1.5 ± 0.1	1.0	19.6		Figures 7, 9, 10
t_{PLZ}, t_{PHZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.6	4.3	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	4.9		
			1.8 ± 0.15	1.5	8.8		
		$C_L = 15$ pF, $R_L = 2k\Omega$	1.5 ± 0.1	1.0	17.6		Figures 7, 9, 10
t_S	Setup Time	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	1.5		ns	Figure 6
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	2.5			
		$C_L = 15$ pF, $R_L = 500\Omega$	1.5 ± 0.1	3.0			
t_H	Hold Time	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	1.0		ns	Figure 6
			2.5 ± 0.2	1.0			
			1.8 ± 0.15	1.0			
		$C_L = 15$ pF, $R_L = 500\Omega$	1.5 ± 0.1	2.0			
t_W	Pulse Width	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	1.5		ns	Figure 5
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	4.0			
		$C_L = 15$ pF, $R_L = 500\Omega$	1.5 ± 0.1	4.0			
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 10)	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		$C_L = 15$ pF, $R_L = 2k\Omega$	1.5 ± 0.1		1.5		

Note 9: For CL = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

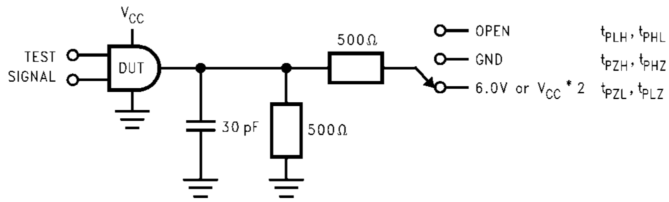
Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	0.15	V
			2.5	0.25	
			3.3	0.35	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	−0.15	V
			2.5	−1.25	
			3.3	−0.35	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	1.5	V
			2.5	2.05	
			3.3	2.65	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$	Units
C_{IN}	Input Capacitance	$V_{CC} = 1.8V$, 2.5V, or 3.3V, $V_I = 0V$ or V_{CC}	6.0	pF
$C_{I/O}$	Output Capacitance	$V_I = 0V$, or V_{CC}, $V_{CC} = 1.8V$, 2.5V or 3.3V	7.0	pF
C_{PD}	Power Dissipation Capacitance	$V_I = 0V$ or V_{CC}, f = 10 MHz $V_{CC} = 1.8V$, 2.5V or 3.3V	20.0	pF

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.15V)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3V ± 0.3V; V_{CC} x 2 at V_{CC} = 2.5V ± 0.2V; 1.8V ± 0.15V
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit

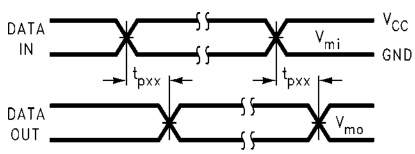


FIGURE 2. Waveform for Inverting and Non-inverting Functions

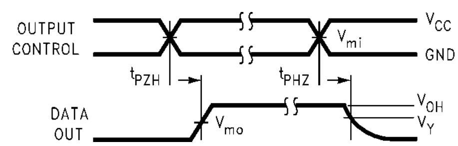


FIGURE 3. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

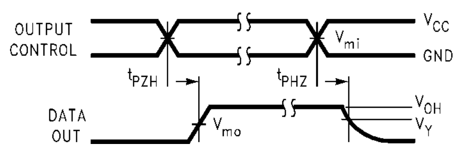


FIGURE 4. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

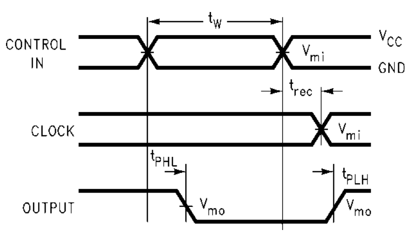


FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms

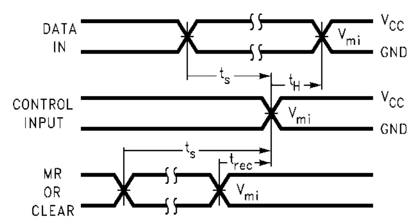
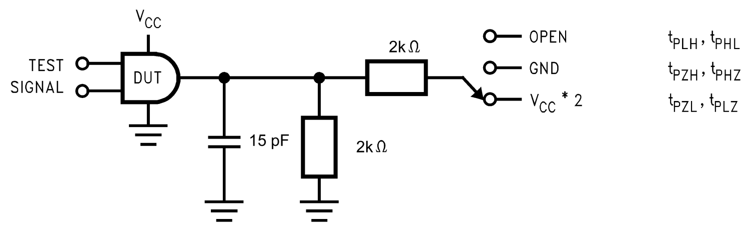


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	**2.5V ± 0.2V**	**1.8V ± 0.15V**
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V

AC Loading and Waveforms (V_{CC} 1.5V ± 0.1V)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC} x 2 at V_{CC} = 1.5V ± 0.1V
t_{PZH}, t_{PHZ}	GND

FIGURE 7. AC Test Circuit

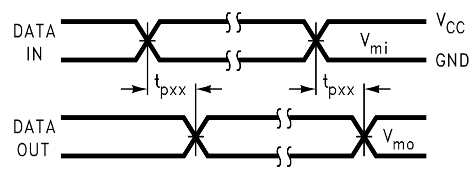


FIGURE 8. Waveform for Inverting and Non-inverting Functions

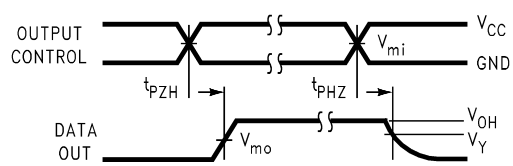


FIGURE 9. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

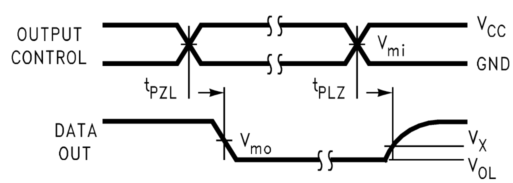
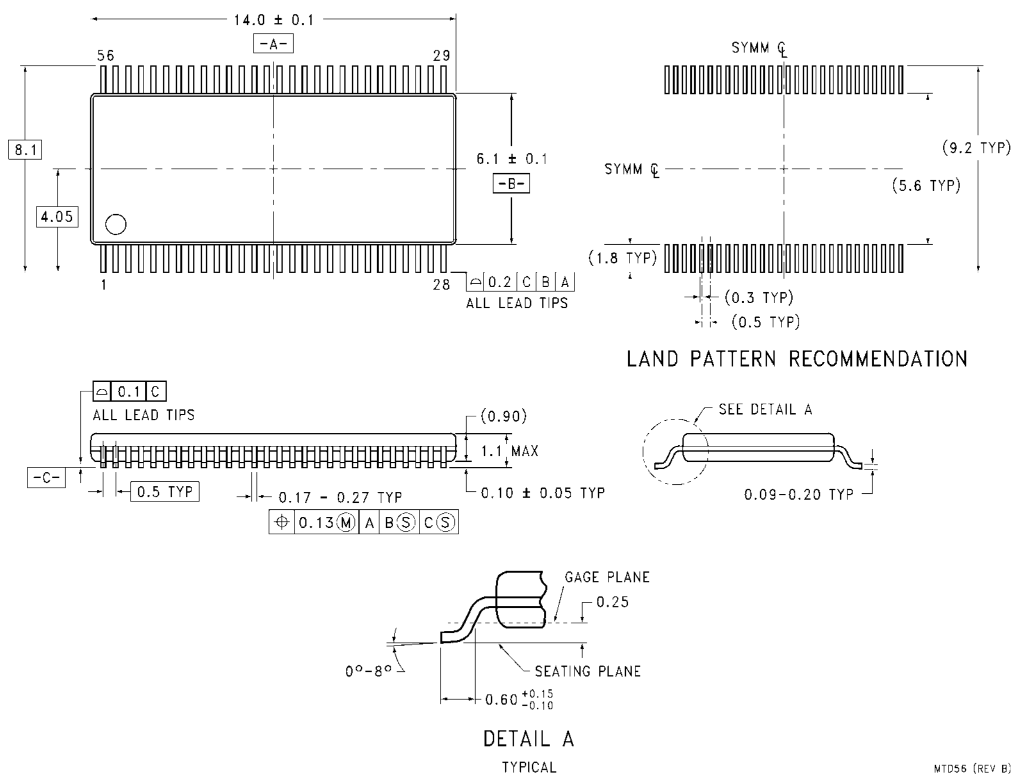


FIGURE 10. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}
	1.5V ± 0.1V
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_X	V_{OL} + 0.1V
V_Y	V_{OH} − 0.1V

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56